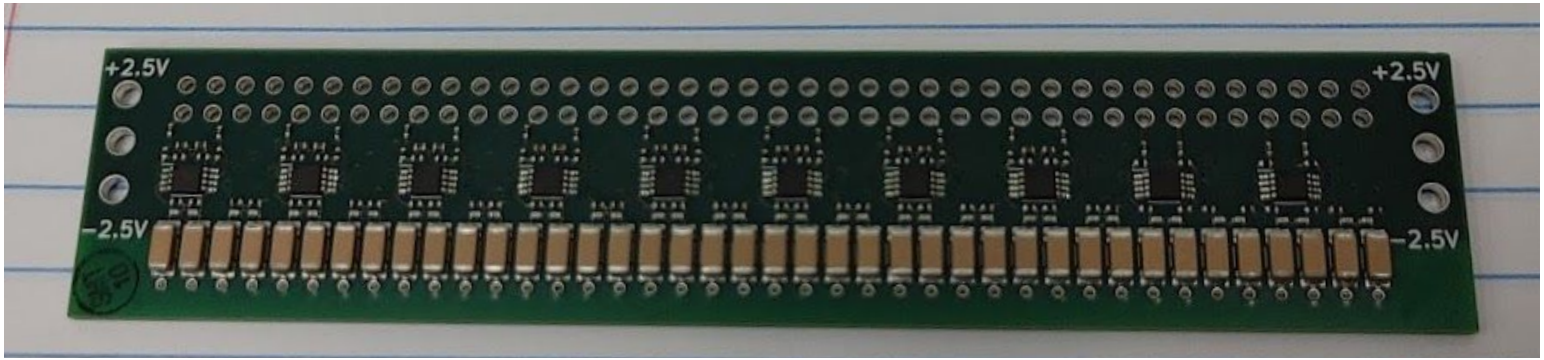
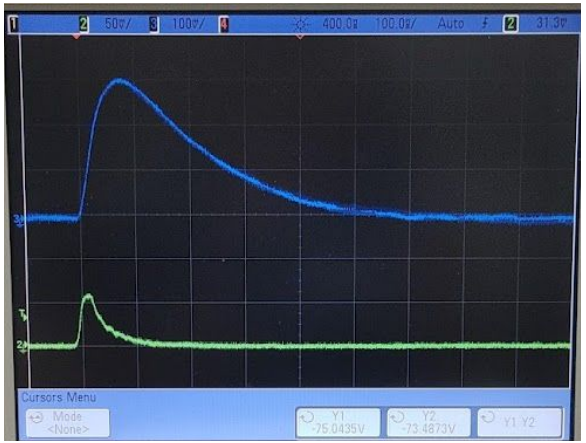
PCB Amplifier Preliminary Results



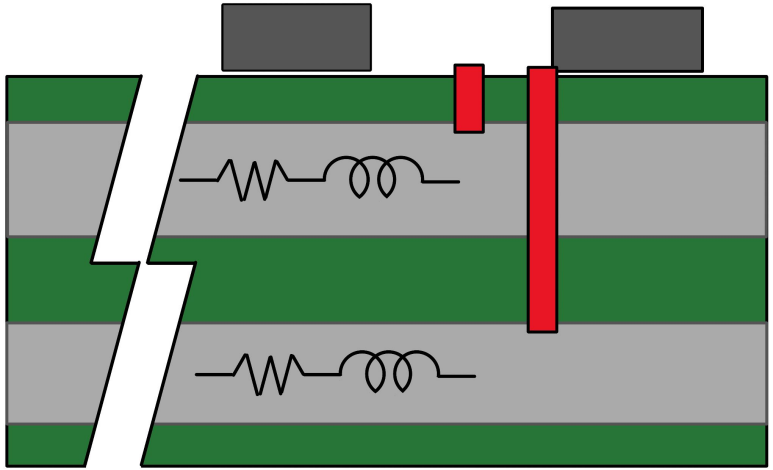
Noise

- Noise present in all amplifier channels
  - 200+ MHz frequency
  - ~200-400 mV peak-peak
  - Easily filtered by oscilloscope low-pass filter
- Noise is notably present in ground and power planes of the PCB
  - Phase relationship between oscillation, probed at various locations, suggests full-board synchronized oscillation…



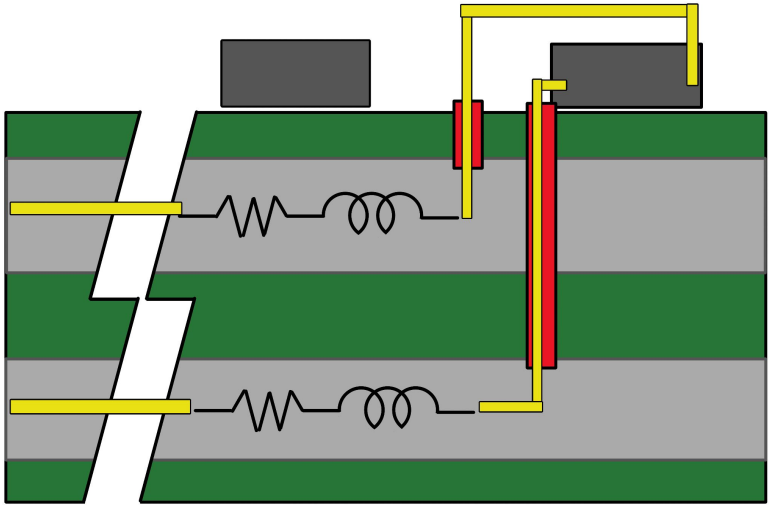
Source of Noise

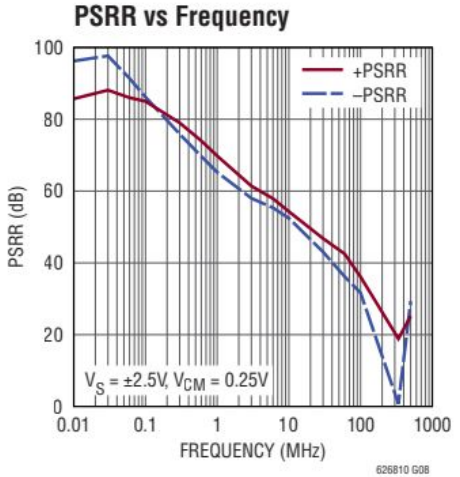
- -2.5V, GND, and +2.5V provided by terminals at board edge
  - Distributed to components through planes
- Parasitic resistances and inductances
  - Naturally present in board



Source of Noise, cont'd

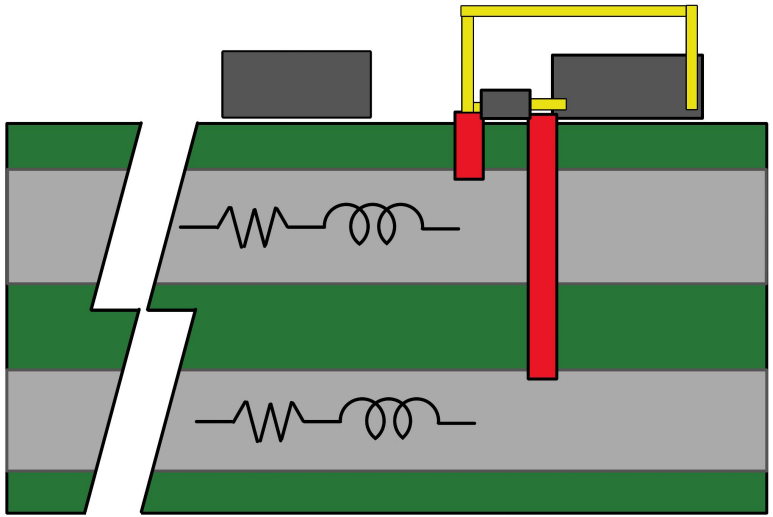
- When transient current is drawn by the op-amp, due to any fluctuation, current must travel to edge of board
  - Natural capacitance between planes is insufficient to source enough current
- Impedance along large loop creates voltage shifts in the ground plane and V+/V- planes
  - Power supply rejection ratio (right) decreases at high frequency
  - All signals are referenced w.r.t ground, thus…
- Feedback loop causing stable oscillation
  - Spans board in-phase (w/ speed-of-light delay)

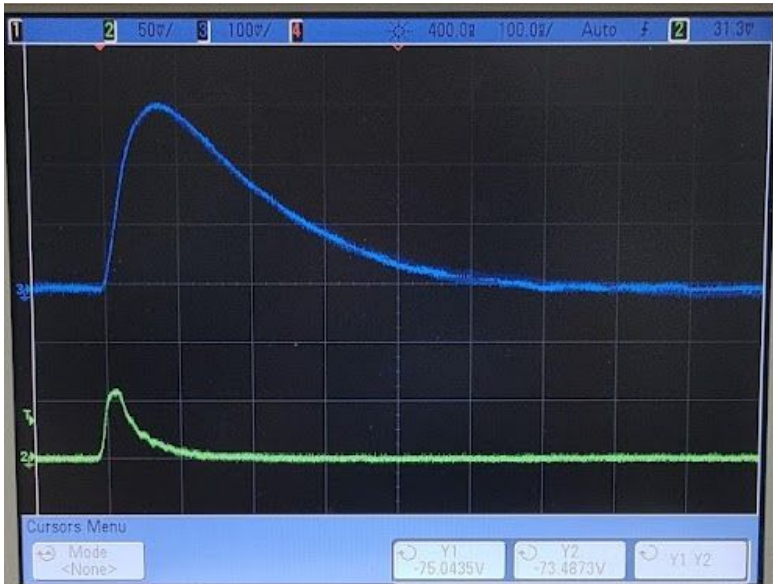




Adding a Decoupling Capacitor

- High capacitance, low series resistance and impedance, capacitor between GND and V+/V- vias
  - Stabilizes planes against transient fluctuations
  - Planes only conduct DC/low frequency current
- Current loop avoids resistive & inductive impedance of planes, preventing feedback and cross-talk of noise

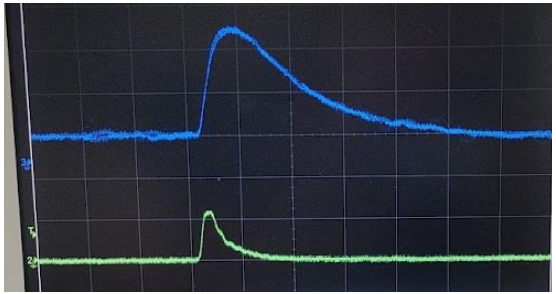




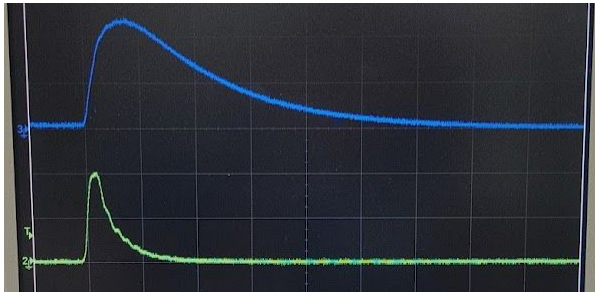
Characterization of Channel Responses

Determining Parasitic Input Capacitance

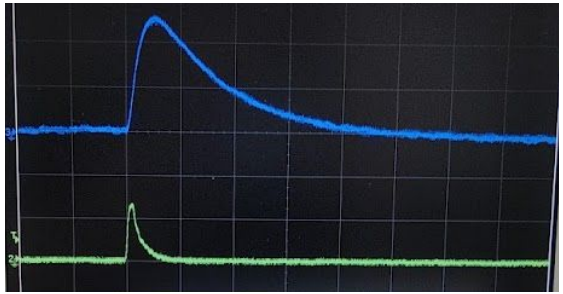
Expected Fall Time Constant (Input Capacitor)	Measured Fall Time Constant (Eff. Total Cap.)
50 ns (2 pF)	130(10) ns (2 + 3.2(4) pF)
100 ns (4 pF)	170(10) ns (4 + 2.8(4) pF)
200 ns (8 pF)	270(20) ns (8 + 2.8(8) pF)
200 ns (16 pF)	240(10) ns (16 + 3.2(8) pF)



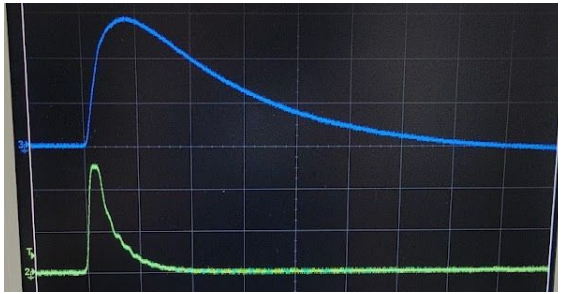
Channel 20



Channel 3



Channel 16



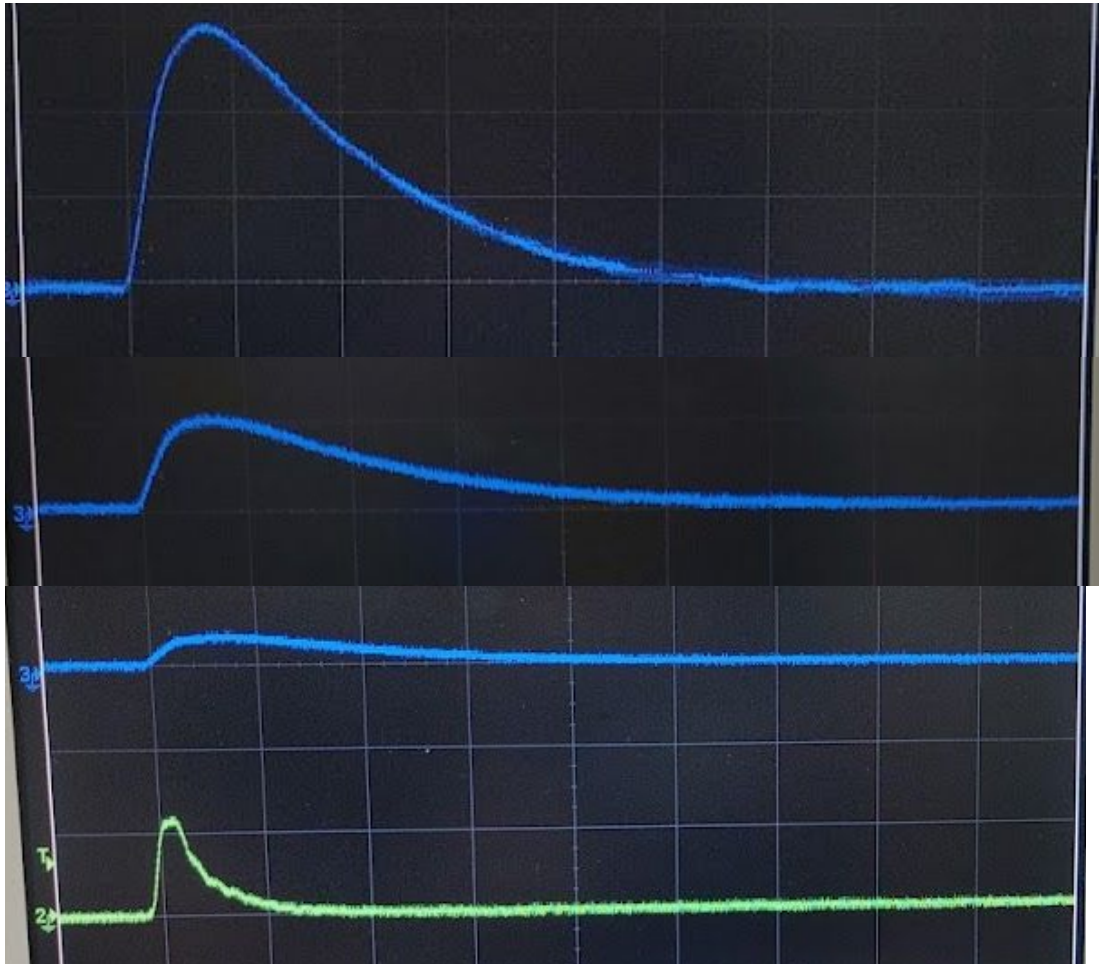
Channel 17

Determining Parasitic Input Capacitance, cont'd

- Thus, parasitic input capacitance ≈ 3.0(3) pF
- LTC 6269-10 op-amp input capacitance specified as ~0.45 pF
- Thus, ~2.5 pF of input capacitance unaccounted for
  - Potential sources include PCB traces, solder pads, input wires to terminals, vias
- Effects of parasitic input capacitance:
  - **Change in the amplifier current-to-pulse-height gain (proportional to $C_{parasitic}/C_{in}$)**
  - Change in falling time constant (proportional to $C_{parasitic}/C_{in}$)
- Thus, may cause some constant offset & some variance between channels, in the amplifier gain
  - Can be minimized by increasing C_{in}, but this imposes other restrictions on gain and shaping

Gain Settings

- Channels 3-5
  - 4 pF C_{in} (+ 3 pF par.)
  - Gains 10x, 33x, 100x
- Gain-Bandwidth product limitation of ~4 GHz
  - In theory, introduces signal delays dependent on gain
  - On order of 0.4 ns, 1.3 ns, 4 ns
  - Initial characterization (right) was 100 ns/div, need further characterization to determine if delays are present
  - Would introduce timing variations dependent on chip-to-chip variation of GBWP



Conclusion

- With reasonably high confidence, oscillatory noise from PCB plane current loops should be dramatically reduced or eliminated by adding decoupling capacitors to the PCB design, located at each op-amp
  - Sustained oscillation requires loop gain > 1, at 400 MHz op-amp gain alone is only 10x
  - Decreasing impedance between V+/V- and ground by even 10x will likely prevent oscillation
- Parasitic capacitance (~3 pF) present on all inputs
  - Can be accounted for in final design
  - Recommend total (discrete + parasitic) input capacitance 6-8 pF, to achieve reasonable gain and resistance to variation due to channel-to-channel differences in parasitic capacitance
- Gain appears to have minimal issues with delays/bandwidth issues
  - Need some further investigation
  - Even with maximum 4 ns delay, a 10% chip-to-chip variance would only create ~0.4 ns variance in event delay